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FOR

METHOD FOR FORMING FLOWABLE DIELECTRIC LAYER IN SEMICONDUCTOR
DEVICE

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1 METHOD FOR FORMING FLOWABLE DIELECTRIC
2 LAYER IN SEMICONDUCTOR DEVICE

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4 Field of the Invention

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6 The present invention relates to a method for
7 manufacturing a semiconductor device; and, more particularly,
8 to a method for forming a flowable dielectric layer by
9 employing a barrier layer on sidewalls of the patterned
10 flowable dielectrics.

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12 Description of the Prior Art
13

14 In recent years, as a semiconductor technology advances,
15 circuit elements and interconnections on a wafer or a
16 semiconductor substrate become increasingly denser and denser.
17 In order to prevent unwanted interactions between these
18 circuit elements, insulator-filled gaps or trenches located
19 therebetween are provided to physically and electrically
20 isolate the elements and conductive lines. However, as
21 circuit densities continue to increase, the widths of these
22 gaps decrease, thereby increasing gap aspect ratios which are
23 typically defined as the gap height divided by the gap width.
24 As a result, it is very difficult to fill these narrow and
25 deep gaps with a predetermined gap-fill material, which can
26 lead to unwanted voids and discontinuities in an insulating
27 layer. Therefore, in attempt to address this problem, there

1 have been proposed techniques for forming the insulating layer
2 by using a material such as a borophosphosilicate glass
3 (BPSG), a high density plasma (HDP) oxide or the like, for
4 improving a gap-fill property of the insulating layer.

5 In general, in case of employing the BPSG as an
6 insulating material, it shows a good gap-fill property but
7 still a drawback that there may be happened the diffusion
8 phenomenon of the dopant in a transistor during a high thermal
9 process, i.e., a reflow process.

10 Meanwhile, an HDP process is recently used to fill high
11 aspect ratio gaps. Typical HDP process employs a chemical
12 vapor deposition (CVD) with a gas mixture containing oxygen,
13 silane, and inert gases such as argon, to achieve a
14 simultaneous dielectric etching and deposition. In the HDP
15 process, an RF bias is applied to a wafer substrate in a
16 reaction chamber. Some of these gas molecules, i.e.,
17 particularly argon, are ionized in the plasma and accelerate
18 toward the wafer surface when the RF bias is applied to the
19 wafer. Material is thereby sputtered when ions strike the
20 surface. As a result, an insulating material deposited on the
21 wafer surface is simultaneously sputter etched to help to keep
22 the gaps open during the deposition process, which allows
23 higher aspect ratio gaps to be filled. Although the HDP
24 process has the aforementioned advantage for filling the high
25 aspect ratio gaps, it suffers from shortcomings that there may
26 be happened etch damages of an underlying layer due to a
27 plasma and further, edges of a micro-pattern are eroded while

1 repeating the deposition and the sputter etch during the HDP
2 process.

3 In attempt to overcome the above problems, therefore,
4 there is proposed another technique utilizing a flowable
5 dielectric for filling the narrow and the deep gaps, i.e., the
6 high aspect ratio gaps, and for protecting the underlying
7 layer from the damage in fabricating the semiconductor device.

8 Referring to Figs. 1A to 1D, there are shown cross
9 sectional views setting forth a conventional method for
10 forming a flowable dielectric layer 120 in a semiconductor
11 device.

12 In Fig. 1A, a semiconductor substrate 110 where an active
13 area 112 and a field area 114 are defined, is prepared in
14 advance by a predetermined process. Thereafter, a plurality
15 of gates 116 with narrow widths are formed on predetermined
16 locations of a top face of the semiconductor substrate 110.
17 Afterward, a predetermined insulating layer (not shown) is
18 formed over the resultant structure and is anisotropically
19 etched into a first predetermined configuration, thereby
20 forming sidewall spacers 118 on the gates 116. Subsequently,
21 a flowable dielectric layer 120 is formed over the resultant
22 structure embracing the gates 116 and the sidewall spacers
23 118.

24 In an ensuing step, referring to Fig. 1B, an annealing
25 process is carried out in a furnace for removing moisture
26 existing in the flowable dielectric layer 120 and densifying
27 the flowable dielectric layer 120. During the annealing

1 process, there is happened a chemical reaction in the flowable
2 dielectric layer 120. That is, silane (SiH_4) and hydrogen
3 peroxide (H_2O_2) are inter-reacted in the flowable dielectric
4 layer 120, to thereby produce Si-O bonds and O-H bonds.
5 Therefore, O-H bonds are again inter-reacted with each other
6 to form a byproduct of water (H_2O) by means of a dehydration
7 reaction. The water produced during the dehydration reaction
8 is removed during the annealing process so that there are
9 formed a plurality of micro-pores 115 in the flowable
10 dielectric layer 120. In particular, a top face of the
11 flowable dielectric layer 120 is shrunk to condense the
12 flowable dielectric layer 120 so that the micro-pores 115 are
13 rarely formed in a top region thereof. However, since a
14 bottom face of the flowable dielectric layer 120 is fixed to a
15 wafer surface, a bottom region of the flowable dielectric
16 layer 120 is hardly shrunk, whereby the micro-pores 115 are
17 formed during the annealing process.

18 After carrying out the annealing process, the flowable
19 dielectric layer 120 is planarized till top faces of the gates
20 116 are exposed by using a method such as a chemical
21 mechanical polishing (CMP).

22 In a next step, referring to Fig. 1C, contact masks (not
23 shown) are formed on predetermined locations of the top face
24 of the flowable dielectric layer 120. Afterward, the flowable
25 dielectric layer 120 is patterned into a second predetermined
26 configuration by using the contact masks as etch masks,
27 thereby forming a plurality of contact holes 101 and patterned

1 flowable dielectrics 120A. In Fig. 1C, it is understood that
2 the micro-pores 115 still remain in the patterned flowable
3 dielectrics 120A.

4 In a subsequent step, a pre-cleaning process is carried
5 out for removing a natural oxide (not shown) formed after the
6 formation of the contact holes 101, thereby securing a bottom
7 area of the contact holes 101. While the pre-cleaning process
8 is performed, the micro-pores 115 are enlarged gradually.
9 That is, the micro-pores 115 formed on the sidewalls of the
10 patterned flowable dielectrics 120A are eroded gradually by a
11 solution for use in the pre-cleaning process. As a result,
12 enlarged micro-pores 115A are formed on the sidewalls of the
13 patterned flowable dielectrics 120A, as shown in Fig. 1C.

14 Following the pre-cleaning process, referring to Fig. 1D,
15 a polysilicon layer is formed over the resultant structure so
16 that the contact holes 101 are filled with the polysilicon and
17 then, is planarized by using a method such as the CMP or an
18 etchback process, thereby forming contact plugs 121 and 122,
19 wherein one contact plug 121 is disposed between the gates 116
20 and the other contact plugs 122 are disposed aside the
21 patterned flowable dielectrics 120A. Since the micro-pores
22 115A became enlarged during the pre-cleaning process, the
23 polysilicon encroaches into the enlarged micro-pores 115A
24 formed on the sidewalls of the patterned flowable dielectrics
25 120A, thereby forming rugged sidewall surfaces 126 of the
26 conductive plugs 122 which are disposed aside the patterned
27 flowable dielectrics 120A.

1 Referring to Figs. 2A and 2B, there are shown micrographs
2 of a scanning electron micrography (SEM) depicting the micro-
3 pores 115 existing in the patterned flowable dielectrics 120A
4 and the conductive plugs 122 having the rugged sidewall
5 surfaces 126.

6 In Fig. 2A, it is understood that the micro-pores 115 are
7 formed in the patterned flowable dielectric layer 120A except
8 the top regions of the patterned flowable dielectrics 120A,
9 after carrying out the annealing process. That is, since the
10 bottom regions of the patterned flowable dielectrics 120A are
11 rarely shrunk during the annealing process, there are
12 inevitably formed micro-pores 115 in the middle and the bottom
13 regions of the flowable dielectric layer 120.

14 Fig. 2B shows the micrograph that the polysilicon
15 encroaches into the enlarged micro-pores 115A after carrying
16 out the pre-cleaning process and the process for forming the
17 polysilicon layer. As aforementioned, the micro-pores 115A
18 formed during the annealing process are enlarged during the
19 pre-cleaning process. Therefore, the conductive plugs 122
20 disposed aside the patterned flowable dielectrics 120A have
21 the rugged sidewall surface 126 encroaching into the patterned
22 flowable dielectrics 120A so that there may be generated a
23 leakage current between adjacent contact plugs, i.e., the
24 bridge phenomenon. Furthermore, as a modern semiconductor
25 device is much more miniaturized, the polysilicon encroaching
26 into the enlarged micro-pores 115A of the patterned flowable
27 dielectrics 120A becomes a serious problem because the modern

1 semiconductor demands dense and miniaturized patterns. Thus,
2 it is difficult to apply the conventional aforementioned
3 process for forming the flowable dielectric layer to the
4 miniaturized semiconductor device having the patterns of the
5 high aspect ratio.

6

7 Summary of the Invention

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9 It is, therefore, an object of the present invention to
10 provide a method for forming a flowable dielectric layer in a
11 semiconductor device by forming a barrier layer on sidewalls
12 of a patterned flowable dielectric, thereby preventing contact
13 plugs encroaching into micro-pores in the patterned flowable
14 dielectric.

15 In accordance with one aspect of the present invention,
16 there is provided a method for forming a flowable dielectric
17 layer in a semiconductor device, the method including the
18 steps of: a) forming a plurality of patterns on a
19 semiconductor substrate, wherein narrow and deep gaps are
20 formed therebetween; b) forming a flowable dielectric layer so
21 as to fill the gaps between the patterns; c) carrying out an
22 annealing process for densifying the flowable dielectric layer
23 and removing moisture therein; d) forming a plurality of
24 contact holes by selectively etching the flowable dielectric
25 layer so as to expose predetermined portions of the
26 semiconductor substrate; e) forming a barrier layer on
27 sidewalls of the contact holes for preventing micro-pores in

1 the flowable dielectric layer; f) carrying out a cleaning
2 process in order to remove native oxides and defects on the
3 semiconductor substrate; and g) forming a plurality of contact
4 plugs by filling a conductive material into the contact plugs.

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6 Brief Description of the Drawings

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8 The above and other objects and features of the present
9 invention will become apparent from the following description
10 of the preferred embodiments given in conjunction with the
11 accompanying drawings, in which:

12 Figs. 1A to 1D are cross sectional views setting forth a
13 conventional method for forming a flowable dielectric layer in
14 a semiconductor device;

15 Figs. 2A and 2B are micrographs of a scanning electron
16 micrography (SEM) depicting the micro-pores existing in the
17 flowable dielectric layer and the conductive plugs encroaching
18 into the micro-pores of the flowable dielectric layer
19 according to the conventional method; and

20 Figs. 3A to 3F are cross sectional views setting forth a
21 method for forming a flowable dielectric layer in a
22 semiconductor device in accordance with a preferred embodiment
23 of the present invention.

24

25 Detailed Description of the Preferred Embodiments

26

27 There are provided in Figs. 3A to 3F cross sectional

1 views setting forth a method for forming a flowable dielectric
2 layer in a semiconductor device in accordance with a preferred
3 embodiment of the present invention.

4 In Fig. 3A, an inventive method begins with preparing a
5 semiconductor substrate 210 obtained where field oxide (FOX)
6 areas 214 and an active area 212 are defined in preset
7 locations of the semiconductor substrate 210 by a
8 predetermined process. Thereafter, gates 216 are formed on
9 predetermined locations of a top face of the semiconductor
10 substrate 210, wherein there is formed a gap between adjacent
11 gates 216 having a narrow space. Afterward, sidewall spacers
12 218 are formed on sidewalls of the gates 216 by using a
13 typical etching process in which the sidewall spacers 218 uses
14 a silicon nitride. As is well known, there are typically
15 formed gate oxides (not shown) beneath the gates 216 and the
16 gates 216 may be a stack structure of a polysilicon layer, a
17 metal layer and a hard mask. Here, the metal layer and the
18 hard mask use tungsten and nitride, respectively.

19 In a next step, a flowable dielectric layer 220 is formed
20 over the resultant structure by using a spin on dielectric
21 (SOD) such as a silicate, a siloxane, a methyl SilsesQuioxane
22 (MSQ), a hydrogen SisesQuioxane(HSQ), an MSQ/HSQ, a
23 perhydrosilazane (TCPS) or a polysilazane. Alternatively, the
24 flowable dielectric layer 220 can be formed by using a low
25 temperature undoped dielectric at a temperature in a range of
26 about -10 °C to about 150 °C under a pressure ranging from about
27 10 mTorr to about 100 Torr, wherein a reaction source uses a

1 mixture gas of $\text{SiH}_x(\text{CH}_3)_y$ ($0 \leq x \leq 4$, $0 \leq y \leq 4$), H_2O_2 , O_2 , H_2O
2 and N_2O . It is preferable that the thickness of the flowable
3 dielectric layer 220 is in the range of about 1,000 μ to about
4 20,000 μ in consideration of heights of the gates 216 and a
5 gap space between the gates 216.

6 After forming the flowable dielectric layer 220,
7 referring to Fig. 3B, an annealing process is carried out in a
8 furnace at a temperature ranging from about 300 μ to about
9 1,000 μ , for densifying the flowable dielectric layer 220 and
10 for removing moisture therein. During the annealing process,
11 there are formed a plurality of micro-pores 215 in the
12 flowable dielectric layer 220. In detail, during the
13 annealing process, there is happened a chemical reaction in
14 the flowable dielectric layer 220. That is, silane (SiH_4) and
15 hydrogen peroxide (H_2O_2) are inter-reacted in the flowable
16 dielectric layer 220, to thereby produce Si-O bonds and O-H
17 bonds. Therefore, O-H bonds are again inter-reacted with each
18 other to form a byproduct of water (H_2O) by means of a
19 dehydration reaction. The water produced during the
20 dehydration reaction is removed during the annealing process
21 so that there are formed a plurality of micro-pores 215 in the
22 flowable dielectric layer 220. In particular, a top face of
23 the flowable dielectric layer 220 is shrunk to condense the
24 flowable dielectric layer 120 so that the micro-pores 215 are
25 rarely formed in a top region thereof. However, since a
26 bottom face of the flowable dielectric layer 220 is fixed to a
27 wafer surface, a bottom region of the flowable dielectric

1 layer 220 is hardly shrunk, whereby the micro-pores 215 are
2 formed during the annealing process.

3 Afterward, the flowable dielectric layer 220 is
4 planarized till the top faces of the gates 216 are exposed by
5 using the CMP process. The reason of carrying out the
6 planarization process before forming contact holes 201 is to
7 secure a wider area in a bottom region of the contact holes
8 201 because an etch profile is slightly inclined toward the
9 bottom faces of the contact holes 201.

10 Subsequently, referring to Fig. 3C, preset contact masks
11 (not shown) are formed on predetermined locations of the top
12 face of the planarized flowable dielectric layer 220.
13 Afterward, the planarized flowable dielectric layer 220 is
14 patterned into a predetermined configuration by using the
15 preset contact masks so as to form the contact holes 201 and
16 patterned flowable dielectrics 220A.

17 Following the formation of the contact holes 201, a pre-
18 cleaning process is carried out for removing a native oxide
19 and defects formed on the semiconductor substrate 210 by using
20 a method such as a wet cleaning or a dry cleaning process.
21 Therefore, it is possible to secure bottom areas of the
22 contact holes 201 without the native oxide and the defects.
23 Like the prior art, the micro-pores 215 on the sidewalls of
24 the patterned flowable dielectrics 220A are gradually enlarged
25 during the pre-cleaning process, thereby forming enlarged
26 micro-pores 215A.

27 Thereafter, referring to Fig. 3D, a barrier layer 226 is

1 formed on bottom faces and sidewalls of the patterned flowable
2 dielectrics 220A and the bottom faces of the contact holes 201
3 with a thickness in the range of about 20 μ to about 300 μ for
4 preventing a gas or a solution infiltrating into the micro-
5 pores in the patterned flowable dielectrics 220A. Herein, the
6 barrier layer 226 uses a material such as a silicon nitride, a
7 silicon oxide, a silicon carbide or the like.

8 After the formation of the barrier layer 226, referring
9 to Fig. 3E, portions of the barrier layer 226 formed on the
10 top faces of the patterned flowable dielectrics 220A and the
11 bottom faces of the contact holes 201 are removed by using a
12 dry etching process, e.g., a blanket etch process. Therefore,
13 the barrier layer 216 exists only on the sidewalls of the
14 patterned flowable dielectrics 220A. Thereafter, a post-
15 cleaning process is carried out for removing another native
16 oxide and defects formed on the semiconductor substrate 210 by
17 using a method such as a wet cleaning or a dry cleaning
18 process. In the present invention, there is introduced the
19 barrier layer 226 before forming contact plugs 221 and 222, it
20 is possible to prevent the micro-pores existing on the
21 sidewalls of the patterned flowable dielectrics 220A being
22 enlarged during the post-cleaning process. Accordingly, the
23 polysilicon in the contact plugs 221 and 222 does not encroach
24 into the enlarged micro-pores 115A of the patterned flowable
25 dielectrics 220A so that a bridge between the adjacent contact
26 plugs 221 and 222 can not be generated.

27 Afterward, referring to Fig. 3F, a conductive layer such

1 as the polysilicon is deposited over the resultant structure
2 and is planarized by using a method such as the CMP process or
3 an etchback process, thereby forming the contact plugs 221 and
4 222. Among the contact plugs 221 and 222, one of the contact
5 plugs 222 serves as a storage node contact plug and the other
6 contact plug 221 serves as a bit line contact.

7 As described above, in comparison with the prior art
8 method, the barrier layer 226 is formed on the sidewalls of
9 the patterned flowable dielectrics 220A before carrying out a
10 post-cleaning process. Therefore, the polysilicon in the
11 contact plugs 221 and 222 can not diffuse into the micro-pores
12 in the patterned flowable dielectrics 220A. As a result, the
13 bridge phenomenon between adjacent contact plugs 221 and 222,
14 which is a serious problem in the prior art method, is
15 effectively prevented.

16 Furthermore, the formation of the flowable dielectric
17 layer 220 is carried out at a low temperature, thereby
18 preventing the diffusion of the dopant in a transistor.
19 Additionally, since the barrier layer 226 is employed before
20 the process for forming contact plugs 221 and 222, it is
21 possible to secure a cleaning process margin, to thereby
22 enhance a contact resistance and remove defects existing in a
23 wafer produced during the etch process easily.

24 While the present invention has been described with
25 respect to the particular embodiments, it will be apparent to
26 those skilled in the art that various changes and
27 modifications may be made without departing from the scope of

1 the invention as defined in the following claims.